What is claimed is:

1. A stacked gate flash memory cell, comprising:

a substrate having a trench therein;

a conductive layer disposed on the bottom of the trench;

a pair of source regions, each disposed in the substrate adjacent to one sidewall of the trench and electrically connected by the conductive layer;

a source isolation layer disposed on the conductive layer;

a pair of tunnel oxide layers, respectively disposed on one sidewall of the trench and the source isolation layer;

a U-shaped floating gate disposed on the source isolation layer, contacting the tunnel oxide layers thereby;

a pair of control gate spacers, respectively disposed on each vertical portion of the U-shaped floating gate, substantially having the same width as the vertical portions;

a U-shaped inter-gate dielectric layer disposed on the U-shaped floating gate and the control gate spacers;

a control gate disposed in the U-shaped inter-gate dielectric; and

a drain region disposed in the substrate adjacent to the trench.

2. The cell as claimed in claim 1, wherein the substrate is P-type silicon substrate.

3. The cell as claimed in claim 1, wherein a bottom insulating layer is further disposed under the conductive layer.

4. The cell as claimed in claim 3, wherein the bottom insulating layer is silicon dioxide.

5. The cell as claimed in claim 1, wherein the conductive layer is N-type dopant doped polysilicon.

6. The cell as claimed in claim 1, wherein the source isolation layer is silicon dioxide.

7. The cell as claimed in claim 1, wherein the tunnel oxide layer is silicon dioxide.

8. The cell as claimed in claim 1, wherein the U-shaped floating gate and the control gate are N-type dopant doped polysilicon.

9. The cell as claimed in claim 1, wherein the U-shaped inter-gate dielectric layer is silicon dioxide.

10. The cell as claimed in claim 1, wherein the control gate spacer is silicon.

11. A method of fabricating stacked gate flash memory cells, comprising the steps of:

providing a substrate;

forming a plurality of parallel long trenches along a first direction in the substrate;

forming a conductive layer and a pair of source regions on the bottom of each long trench, wherein the source regions are respectively disposed in the substrate adjacent to two sidewalls of each long trench and electrically connected by the conductive layer therein;

forming a source isolation layer on each conductive layer;

forming a tunnel oxide on two sidewalls of each long trench;

forming a U-shaped floating gate on each source isolation layer, contacting the tunneling oxide layers;

forming a pair of control gate spacers respectively disposed on the vertical portion of the U-shaped floating gate, substantially having the same width as the vertical portions;

forming an U-shaped inter-gate dielectric layer on each U-shaped floating gate and the control gate spacers;

forming a control gate in each U-shaped inter-gate dielectric layer;

forming a plurality of parallel shallow trench isolation (STI) regions along a second direction, defining a plurality of cell trenches; and

forming a drain region in the substrate adjacent to each cell trench.

12. The method as claimed in claim 11, wherein the first direction is perpendicular to the second direction.

13. The method as claimed in claim 11, wherein the substrate is P-type silicon substrate.

14. The method as claimed in claim 11, further comprising before forming a plurality of parallel long trenches along a first direction in the substrate, the step of sequentially forming a pad oxide layer and a mask layer on the substrate.

15. The method as claimed in claim 14, wherein the mask layer is silicon nitride.

16. The method as claimed in claim 14, wherein the pad oxide layer is silicon dioxide.

17. The method as claimed in claim 11, further comprising before forming a conductive layer and a pair of source regions on the bottom of each long trench, the step of forming a bottom insulating layer on the bottom of each long trench.

18. The method as claimed in claim 11, wherein forming a conductive layer and a pair of source regions on the bottom of each long trench further comprises the steps of:

forming a source material layer in each long trench;

performing a thermal annealing process on the source material layer, driving out dopants therefrom, forming a pair of source regions in the

substrate adjacent to two sidewalls of each long trench, electrically connected by the conductive layer therebetween; and

removing the source material layer from each long trench.

19. The method as claimed in claim 18, wherein the source material layer is N-type doped polysilicon.

20. The method as claimed in claim 19, wherein the N-type doped polysilicon comprises phosphorous (P) doped polysilicon or arsenic (As) doped polysilicon.

21. The method as claimed in claim 11, further comprising before forming a tunnel oxide on two sidewalls of each long trench, the step of performing a threshold voltage implantation on the sidewalls of each long trench.

22. The method as claimed in claim 11, wherein forming a U-shaped floating gate on the source isolation layer, contacting the tunnel oxide layers further comprises the steps of:

conformably depositing a floating gate layer in each long trench;

forming a protective layer on the floating gate layer in each long trench, exposing portions of the floating gate layer; and

removing portions of the floating gate layer exposed by the protective layer, forming a U-shaped floating gate therein.

23. The method as claimed in claim 22, wherein the protective layer is boro-silicate-glass (BSG).

24. The method as claimed in claim 11, wherein forming a pair of control gate spacers, each disposed on the vertical portion of the U-shaped floating gate, having the same width as the vertical portions further comprises the steps of:

conformably depositing materials of a control gate spacer layer;

etching the materials of the control gate spacer layer, stopping at the protective layer in each long trench, forming a control gate spacer disposed on each vertical portion of each U-shaped floating gate, substantially having a same width as that thereof; and

removing the protective layer therein.

25. The method as claimed in claim 24, wherein the method for removing the protective layer is wet etching.

26. The method as claimed in claim 25, wherein the control gate spacer is silicon dioxide.

27. The method as claimed in claim 11, wherein forming a plurality of parallel shallow trench isolation (STI) regions along a second direction, defining a plurality of cell trenches, further comprises the steps of:

sequentially performing photolithography and etching, defining a plurality of parallel long

isolation trenches along a second direction, stopping at the source isolation layer therein; and

forming an insulating layer in each long isolation trench.

28. The method as claimed in claim 27, wherein the insulating layer is silicon dioxide.

29. The method as claimed in claim 27, wherein the method of forming the insulating layer is high density plasma enhanced chemically vaporization deposition (HDP CVD).

30. The method as claimed in claim 12, wherein forming a drain region in the substrate adjacent to each of the cell trenches further comprises the steps of:

removing the mask layer, exposing the pad oxide layer;

performing a drain implantation;

performing a thermal annealing process, forming a drain region in the substrate adjacent each cell trenches;

removing the pad oxide layer; and

forming a second insulating layer on each drain region.

31. The method as claimed in claim 30, wherein impurities used in the drain region implantation are N-type impurities.

32. The method as claimed in claim 31, wherein the N-type impurities comprise phosphorous (P) ions or arsenic (As) ions.

33. The method as claimed in claim 30, wherein the method for forming the second insulating layer is low pressure chemical vapor deposition (LPCVD).